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CMS pixel detector upgrade

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ABSTRACT: Starting in 2013, the Large Hadron Collider (LHC) accelerator at CERN will deliver an increased luminosity, with an eventual goal of reaching $10^{35} cm^{-2}\ s^{-1}$, to the Compact Muon Solenoid (CMS) experiment. This increase will happen in two steps creating far reaching implications for the CMS detector, especially for the tracking system. The first step, Phase I, will double the LHC luminosity and only the pixel tracker detector will be replaced. The second step, Phase II or SLHC, will require a new granularity of the strip detector which should substitute its strips with short strips or 'strixels'. SLHC will also provide an unprecedented track rate and radiation level that demands a completely new readout architecture.

This paper addresses these challenges, focusing on the replacement of the CMS inner pixel detector for Phase I and shows the status of the activities.

KEYWORDS: Particle tracking detectors; Radiation damage to detector materials (solid state); Electronic detector readout concepts (solid-state)

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1 Introduction

The Compact Muon Solenoid, CMS, is a general purpose detector for the Large Hadron Collider, LHC, accelerator at CERN [1]. It consists of 4 parts. Starting from the interaction point, it has a tracking system based on silicon sensors segmented into pixels in the innermost region and into strips in the outermost one; the tracker provides the measurement of charged particle momentum; an electromagnetic and hadronic calorimeter measure the charged and neutral particle energies; a superconducting magnet provides a 4T magnetic field; the iron yoke for the flux-return and a muon system that surrounds the magnet.

All the different parts were optimized in order to match the physics requirements during the LHC operations. LHC provides CMS with $p-p$ interactions at an energy of $14\,TeV$ with a collision frequency of 25 ns, peak luminosity of $10^{34} cm^{-2}\ s^{-1}$ and integrated luminosity of $100\ fb^{-1}/year$ [2].

To extend significantly the physics potential of the LHC a luminosity upgrade is already scheduled for 2013. The first increase of the luminosity by a factor of 2 (Phase I) will be obtained by pushing the current accelerator capabilities to its ultimate. For the second increase, SLHC project, new accelerator magnets will bring the luminosity to $10^{35} cm^{-2}\ s^{-1}$ [3].

The CMS detector performance will be dramatically affected, in particular close to the interaction point where the pixel detector is located. The current pixel detector consists of 3 barrel layers, which are at 4.4 *cm*, 7.3 *cm* and 10.2 *cm* from the beam center, and two forward pixel disks on either end of the barrel at a distance of 34.5 *cm* and 46.5 *cm* from the barrel center.

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Two challenges, among the many created by the new luminosity scenarios, are: the high track rate and the high level of radiation. The former applies to the architecture of the readout electronics, the latter mainly affects the charge collection properties of the detector.

After 2-3 years of operating at LHC the performances of the innermost barrel layer sensors will degradate significantly due to radiation damage. For this reason a replacement of the whole pixel detector is scheduled for 2013 in conjunction with the shutdown for Phase I upgrade. This intervention will allow the deployment of a new readout, suitable for the increased luminosity, and a lighter structure to reduce the tracker material budget.

The SLHC upgrade, that should start around 2018, will require a new granularity of the tracker detector. An additional 4th pixel barrel layer and a 3rd pixel disk will need to be added. The silicon strip tracker will replace at least part of the detector with short strips or 'strixels' and need a new tracker readout architecture.

The constraints for both cases will be to: (1) achieve similar performance in momentum resolution and track reconstruction efficiency, (2) keep the material budget at the same or a lower level, and (3) use the existing power cables, optical fibers and cooling tubes that connect the pixel detector with power supplies and the data acquisition system in the service cavern.

This paper focuses only on the Phase I upgrade describing briefly the pixel detector inefficiencies due to the higher luminosity. A review of the recent Research and Development activities is also given. A summary table with the possible scenarios for the pixel detector replacement for Phase I is reported at the end of the paper.

2 Pixel detector limitations due to higher luminosity

The innermost pixel barrel layer, while operating at the full LHC luminosity, is already at the efficiency limit: it is expected that the data loss will be 4% due to the pixel readout chip occupancy and that the position resolution will degrade due to silicon sensor radiation damage. In addition, the present tracker material budget reduces up to 10% the tracking reconstruction efficiency of high momentum particles due to nuclear interactions.

Increasing the luminosity, even if only by a factor of 2, will increase the event rate and consequently both the occupancy of the readout electronics and the radiation damage. In this section the current detector inefficiencies are quantified and the possible improvement that can be achieved for Phase I are listed.

2.1 Silicon sensor limitations

The actual CMS Pixel sensor consists of n type silicon substrates with $n+$ pixelized implants, the distance between $n+$ implants is 20 μm (Gap). The inter-pixel isolation is provided by p implant structures (moderated p-spray in the barrel and p-stops in the forward) that surround the pixels. The substrate material is standard FZ material enriched with oxygen atoms diffused on the wafer (DOFZ) [4].

The particle position reconstruction in pixel detector relies not only on the charge measured by a single pixel but also on the charge shared between pixels. The analog interpolation of the charge between neighboring channels is in fact performed to improve spatial resolution. The charge sharing is enhanced in a magnetic field by the Lorentz deflection for the charge deposited by ionizing tracks.

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Due to radiation damage and after type inversion, the depletion voltage (V_{dep}) increases with the irradiation fluence. Higher depletion voltage means smaller Lorentz angle and then smaller charge sharing in the CMS pixel sensor design. Moreover, irradiation introduces traps in the silicon lattice with a consequent reduction of the total charge [6]. The detector performance degradets steadily with irradiation and for example, at a fluence of $\simeq 6 * 10^{14}\ Neq/cm^2$, although the detection efficiency is still high ($> 90\%$), the cluster are mainly one-pixel and the spatial resolution is therefore expected to be 29 μm [5], exceeding the 20 μm limit necessary for an efficient b-tagging.

These are the main reasons for substituting the pixel sensors after 2–3 years of running of LHC at the highest luminosity when the critical fluence should be reached in the innermost layer [4].

Within the RD50 (Radiation hard semiconductor devices for very high luminosity colliders) and CMS collaborations of CERN, *R&D* studies are ongoing in order to choose the best sensor technology for Phase I. The aim is to maintain the present sensor design and its basic features: $n+$ pixels to collect e^- that are less probable to be trapped, and oxygenated material that has shown a lower increase of the depletion voltage when irradiated with charged particles.

Sensor work is ongoing in the following areas:

1. determine the limits of the present sensors in terms of detection efficiency and charge loss;
2. investigate a slightly modified sensor geometry (Gap=30μm) and smaller guard rings to reduce the sensor dead region between adjacent modules and consequently the geometrical inefficiency;
3. characterize n+ on p sensors as they are cheaper due to production using a single-sided process;
4. characterize intrinsically oxygenated silicon substrates such as Magnetic Czochralski Silicon (MCz) [7].

2.2 Readout chip limitations

The architecture of the readout chip (ROC) was adjusted to the LHC environment as described in ref. [8]. The pixel ROC was originally optimized for modules at a radius of about 7 *cm* from the interaction point and for LHC peak luminosity. The chip was subsequently improved for the readout of the innermost layer modules at peak luminosity. Nevertheless, the first layer is still more inefficient with respect to the others. As the ROC is fabricated in a radiation hard technology, the performance of the readout electronics are basically limited by the readout losses at high rate. The main mechanism for data loss is described in detail in ref. [9] and will be shortly summarized here.

The ROC consists of 4160 pixel cells arranged in 52 columns and 80 rows. The readout in a ROC is arranged in double columns. The information coming from pixels of two adjacent columns are stored in the same buffer at the periphery of the ROC waiting for the accepted LHC level 1 trigger. Each pixel cell is able to measure the amount of charge produced in the sensor, to amplify it, to compare with a threshold and to send it out together with the address of the hit pixel. As soon as the periphery is notified by the hit pixel, it creates a *time stamp* and initiates a scan ("column drain") which copies the amplitude of the hit pixels in the double column into the *data buffer* and then waits for the trigger confirmation.

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	Layer 1	Layer 2	Layer 3
Pixel busy (%)	0.21	0.08	0.04
Double column busy (%)	0.25	0.02	0.004
Data Buffer full (%)	0.17	0.08	0.07
Timestamp Buffer full (%)	0.17	0.001	0
Reset loss (%)	3.0	1.0	0.7
Total (%)	3.8	1.2	0.8

Table 1. Expected inefficiencies in the present readout system estimated at full LHC luminosity (ref. [9]).

A single barrel pixel module consists of 16 or 8 ROCs and a Token Bit Manager (TBM), located on top of the module, that manages the ROC readout. The TBM controls the readout of different ROCs by initiating, for each incoming trigger, a token pass to the first ROC of the group. The first ROC then passes the token bit to the second ROC and the data to the TBM.

High rate tests and Monte Carlo simulations of the Pixel ROC have shown that the main sources of the data loss are due to (ref. [9]):

1. *Pixel busy.* The hit pixel is insensitive to further hits until the charge is transferred to the periphery.

2. *Double column busy.* During the draining mechanism of one double column the readout is still sensitive to further hits, but only two pending column drains are possible while the first drain is ongoing.

3. *Buffer overflow.* The size of both data and time stamp buffer is limited.

4. *Reset loss.* This is the dominant source of data loss caused by the reset of the double column after each triggered readout.

The occurrence probabilities of the different mechanisms of data loss have been evaluated for the present readout system, the expected inefficiencies at the nominal full LHC luminosity are reported in table 1.

As the particle rate is increased, the *Reset loss* increases as well even if not so drastically as it mainly depends on the trigger latency and rate which are assumed to stay constant; on the contrary the *Buffer overflow* becomes critical. For example to keep the *Buffer overflow* loss below 1% at the full Phase I luminosity, $2 * 10^{34} cm^{-2}\ s^{-1}$, the buffers have to be increased by a factor of 2 [9].

In order to improve the rate capability of the pixel modules and allow the operation at higher luminosity some modifications to the ROC are considered. The short time scale cannot allow dramatic modification to the readout architecture. A redesign of the ROC to double the buffer sizes is possible in the current 0.25 μm technology, and will be pursued for Phase I.

2.3 Material budget contribution

The services, support structure and cables of the silicon tracker introduce a non-negligible amount of material into the tracking volume that reduces the track reconstruction efficiency mostly because of nuclear interactions. The tracker material, and consequently this loss, depends on the rapidity

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(η) region considered. For example, while for muons the track reconstruction efficiency is close to 100% in most of the pseudorapidity range, for pions it drops to 95% at $\eta \simeq 0$ and up to 90% at $\eta \simeq 1.5$.

All the power and signal cables from the pixel barrel detector (figure 1 and 2 in [10]) are routed to the two end-flanges, behind both ends of the barrel region, and then directed to an optical link system that converts the electrical signals into optical. The signal is then sent over a 2 *m* optical fiber towards the end of the strip tracker system where the CMS Tracker patch panel is located.

In the central region, $\eta < 1.2$, the main contribution to the material budget comes from silicon sensors, ROCs, carbon fiber mechanical structure, cooling pipes and kapton cables. While for $\eta > 1.2$ the main contribution is due to the cooling manifolds, the complex and heavy PCB end-flange print with more then 800 plugs, the kapton cables and the optical mother boards. In addition the cooling manifolds and the PCB end-flange are directly in front of the first forward pixel disk. This material in unit of radiation length was evaluated as function of pseudorapidity considering tracks coming from the interaction point with a smeared primary vertex in *z* of one sigma (7.5 *cm*). The fractional radiation length is around 0.05 at $\eta = 0$, increases up to 0.1 at $\eta = 1.1$, and has a maximum of 0.19 at $\eta = 1.7$ and then decreases with η [13].

Ideas for Phase I, that could also be solutions for SLHC, are listed here based on the material budget savings priority:

1. *CO_2 cooling*. Substitute the present mono phase C_6F_{14} with a bi-phase CO_2 cooling fluid. The CO_2 is lighter; its density is $\simeq 1.03 g/cm^3$ compared to $1.76 g/cm^3$ of C_6F_{14}. Moreover, CO_2 allows long cooling loops ($\simeq 2-3$ *m*) with very small diameter pipes ($\simeq 1$ *mm*) and the possibility to serialize the pipes with a negligible pressure drop. On the contrary, the present coolant has parallel cooling pipes with manifolds and large diameter silicon hoses in front of forward pixel disks.
2. *μ-twisted pair cables*. Substitute the kapton cables with a μ-twisted pair cable. This new cable is lighter and will allow the transmission of the electrical signals over a distance of about 2 *m*, allowing to move the print and the optical link system further back towards the CMS Tracker patch panel (shift to larger η) [12].
3. *New lighter pixel modules*. Use smaller HV-capacitor on the HDI, reducing the ROC thickness from $175\mu m$ to $75\mu m$ and installing the module directly on the mechanical structure eliminating the carbon fiber basestrips that support the sensor. The lighter module production and the bump-bonding of the thinner chips has to be developed and verified [13].
4. *Digital, serial and fast readout*. Incorporate more functionality into the ROC chip in order to have a digital readout at a frequency of 320 *MHz* and serialize the communication lines. The new link will reduce drastically the number of lines and connections. A new version of the readout chip has to be implemented [12].
5. *New mechanical structure*. A new simplified mechanical design has been presented which includes the new pipes for CO_2 cooling. It also includes a 4^{th} barrel pixel layer and a 3^{rd} forward disk in order to provide 4 pixel hits over most of the tracker's rapidity region. Even if this is not required for Phase I, a 4-layer mechanical structure can be delivered for 2013 ready to be populated with pixel modules for SLHC.

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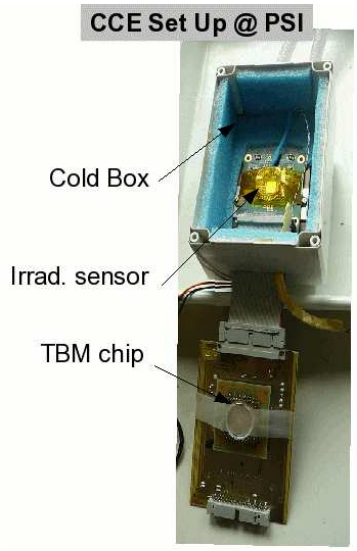


Figure 1. CCE experimental setup.

3 *R&D* activities for Phase I upgrade

Different *R&D* activities have been started in the CMS pixel community in view of the replacement of the pixel detector for Phase I.[1]

3.1 Silicon sensors for high doses

The radiation fluence expected in the innermost layer of the barrel pixel detector in one year of LHC running at peak luminosity is around $3 * 10^{14}\ Neq/cm^2$. Doubling the luminosity will double this value. High dose irradiation tests have been performed to establish the maximum radiation level that can still be used with the present pixel technology.

Single silicon chips (with 4160 pixels) from the production wafers of the CMS barrel pixel detector have been bump-bonded to readout ROCs and irradiated with positive pions up to $6 * 10^{14} Neq/cm^2$ at PSI and with protons up to $5 * 10^{15} Neq/cm^2$ at CERN. The goal is to measure the charge collection efficiency as a function of bias voltage and irradiation fluence. The detailed results of this study, carried on at PSI during Summer 2008, are reported in ref. [11].

The experimental setup (figure 1) consists of a silicon irradiated chip under test, a cold box that keeps the temperature fairly constant at $T \simeq -10°C$ and a Sr-90 source. The readout is provided by a slightly modified standard readout system used for the CMS barrel pixel module testing: for the single ROC readout, the TBM is located on an external PCB board as shown in figure 1). Before data is taken, a calibration of the ROC parameters, as defined for the barrel module test [15], has to be performed.

[1]This section describes in particular the projects which are ongoing at the Paul Scherrer Institute (PSI Villigen, Switzerland) in collaboration with the PSI-CMS pixel group and the five US Universities: University of Kansas, Kansas State, University of Nebraska Lincoln, University of Illinois Chicago and University of Puerto Rico Mayaguez, within a project funded by the US National Science Foundation titled "PIRE: Collaborative research with the Paul Scherrer Institute and Eidgenssische Technische Hochschule on Advanced Pixel Silicon Detectors for the CMS detector".

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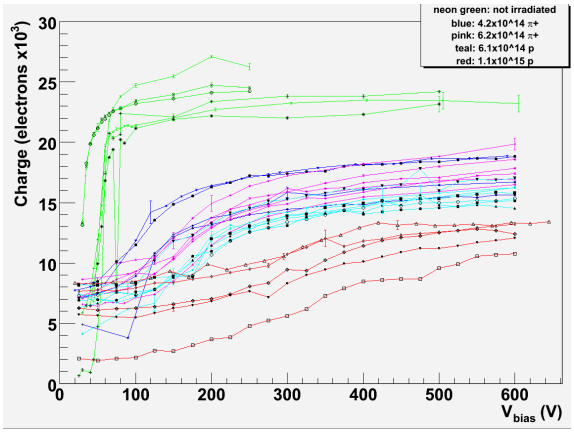


Figure 2. Charge on irradiated sensors.

In figure 2 the charge of single pixel clusters measured on different irradiated sensors and on some unirradiated ("neon green") for comparison, is reported as a function of the bias voltage. The maximum charge measured in an unirradiated sensors is around 23000 e^- as expected for a MIP in 300μm of silicon. For irradiated sensors the ROC calibration and the charge measurement was possible up to a fluence of $1.1 * 10^{15} Neq/cm^2$. The charge measured decreases with fluence as expected and, at the highest fluence, is slightly above 10000 e^- that is around 50% of the non-irradiated ones. For fluences higher than $1.1 * 10^{15} Neq/cm^2$ the most probable value of the charge collected in the silicon sensor is lower than the threshold of the comparator. Ongoing studies focus on defining a new ROC calibration procedure that will allow lowering the comparator threshold and cutting the noise, that increases with the fluence. An improved set up with a scintillator trigger is also planned in order to measure the readout efficiency.

3.2 New fast readout link

As discussed in paragraph 2.3 an important contribution to the tracker material budget comes from the PCB end-flange print, the kapton cables and the optical mother boards located between the end of the pixel barrel and the first forward disk. A large improvement can be made if this material could be moved further back (2 m) outside of the tracking volume and the kapton cables could be replaced with thinner wires. A schematic view of this new concept is drawn in figure 3.

This solution will reduce both the number of plugs and connections at the end-flange (End Ring in the picture). To minimize the material budget a μ-twisted pair of unshielded, Copper Cladded Aluminum (CCA) wires are under investigation; to minimize the power consumption a low differential signal level should be used.

To communicate with the module several signal are transmitted: the clock, trigger, control and data. The data format for the present ROC analog signal consists of 6 levels for the pixel address and 1 analog signal for the pixel charge.

The idea is to substitute each differential line on the kapton cable, used for the parallel transmission of the signals, with a μ-twisted pair cable and maintain the analog readout of the data signal.

A further improvement, to minimize the wiring effort of the parallel lines, would be to use a serial data link. In the latter case the different signals: clock, trigger, controls and data should

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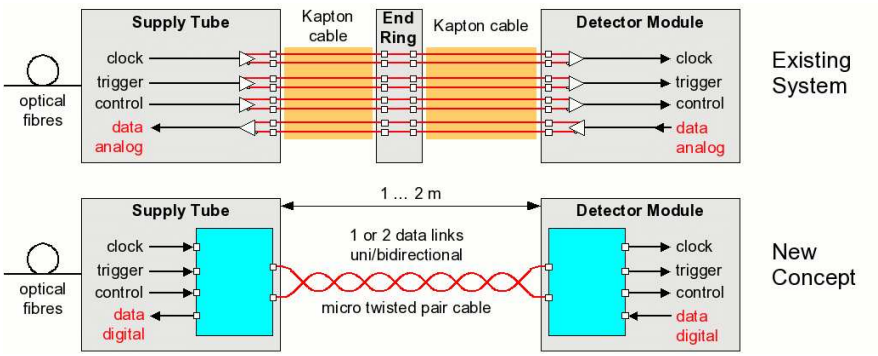


Figure 3. Signal connection between the pixel module and the optical link system: present concept (top), new concept with μ-twisted pair cable (bottom).

be serialized on the same high speed 160 or 320 Mbit/s (multiple of the 40 *MHz* LHC clock frequency) line. The new serial link has to be fully digital: no analog pulses can be transmitted. For this solution an ADC to digitize the pulse height has to be implemented in the ROC. In this scenario the clock line can be avoided since the clock can be regenerated from the signal.

Studies are underway to check whether the communication of the analog and/or digital signals between the detector and the optical system is feasible using thinner and longer cables. First, a complete characterization of the new cable in terms of impedance, signal loss and quality, bit error rate, cross talk and high frequency transmission is needed. Second, the teal square blocks in figure 3 need to be expanded. A new digital protocol should be defined and tested. New circuits like PLL clock recovery, the PLL clock multiplier, and the on-chip ADC should be developed.

A test chip has been designed at PSI with all the components needed for the cable tests. The test chip description and the first encouraging results of the new 160/320 MHz, 2*m*, serial link are described in ref. [12].

It has been shown that communicating at high frequency with the μ-twisted pair cable is possible. Moreover, this line (even if unshielded) is not affected by the crosstalk and the bit error rate at 80 $Mbit/s$ is below 10^{-11}.

The electrical characteristics of the cable have also been measured: the differential impedance is $48 \pm 2\Omega/m$ and the power loss is about 50% for a wire of 2m length, in agreement with the calculations.

4 Possible scenarios for Phase I upgrade

The possible scenarios for the barrel pixel detector upgrade for Phase I are described in [14] and summarized in table 2. In column "Weight" the weight of one half barrel pixel detector is estimated considering: modules, power cables and plugs, prints, cooling manifolds and pipes and colling fluid in tubes. The last column, "Start Date", shows the period where the *R&D* activities should start to be ready for 2013.

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Option	Layer/ # of modules	Cooling	ROC	ReadOut speed	Power	Weight	Start Date
0	3/768	C_6F_{14}	as now	as now	as now	3921 *gr*	Aug 2010
1	3/768	C_6F_{14}	**2xbuffer**	as now	as now	3921 *gr*	Nov 2009
2	3/768	**CO_2**	2xbuffer	as now	as now	2274 *gr*	Nov 2009
3	3/768	CO_2	2xbuffer	analog 40 *MHz* **μ-twisted pairs**	as now	1624 *gr*	Nov 2009
4	3/768	CO_2	2xbuffer **ADC**	**digital/serial** 320 *MHz* μ-twisted pairs	as now	1267 *gr*	Dec 2008
5	**4/1428**	CO_2	2xbuffer ADC	digital/serial 320 *MHz* μ-twisted pairs	**DC-DC step down converter**	$\simeq$ 2400 *gr*	possible for 2013?

Table 2. Possible scenarios for Phase I upgrade.

"Option 0" is very conservative: rebuild exactly the same detector with minimum effort but also with the same inefficiencies.

In "Option 5", populate the 4th barrel layer would be possible only if the Phase I start up is delayed and if a high speed serial readout link and a voltage step down converter can be used. This is, in fact, the only way to serve the increased number of modules with the present number of optical fibers and power cables.

"Option 1", doubling the buffer size, could be done now.

"Option 2", CO_2 cooling system, is well advanced and could be possible.

The encouraging results for the new link make "Option 3" possible, while the feasibility of "Option 4" still has to be proven.

5 Conclusion

The scheduled increase of LHC luminosity has implications for the CMS detector especially for the tracking system closer to the interaction region. For the first luminosity upgrade only the pixel system will be substituted, while for the SLHC, a new geometric design could be made for the whole tracker and a new readout architecture is needed. For both detector upgrades stringent conditions imposed by the CMS infrastructure have to be considered.

The present activities in the CMS pixel collaboration are on the first upgrade focusing on the different possibilities listed in table 2. A minimum upgrade of the ROC readout and a slight modification of the sensor technology towards radiation harder silicon sensors are foreseen. The new mechanical design and studies on the CO_2 cooling have already started. Further improvements, such as using μ-twisted pair cables for the analog or digital readout are still considered. Building and populating the 4th barrel layer would only be possible if the Phase I start up is delayed and high speed serial readout link and a voltage step down converter are developed.

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